Notice of Allowability	Application No.	Applicant(s)	
	10/718,975	VU, HA CHU	
	Examiner	Art Unit	
	Stephen G. Sherman	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed the 23 April 2007*.

2. ☒ The allowed claim(s) is/are *1,2,4-16,18-20 and 27-37*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Davin Chin on 18 May 2007.

2. The application has been amended as follows:

Please amend claim 1 as follows:

1. An interface circuit for processing an input signal comprising:

a phase locked loop (PLL) circuit adapted to generate a plurality of phased signals from a synchronizing signal that is associated with the input signal, wherein the PLL is arranged to provide each phased signal of the plurality of phased signals on at least one corresponding separate signal line of a plurality of signal lines;

a phase adjuster including:

a first phase selector for selecting a first one of the phased signals;

a second phase selector for selecting a second one of the phased signals; and

a phase mixer for multiplying the first selected phased signal with a first weight, multiplying the second selected phased signal with a second weight, and adding together the first and the second multiplied phased signals to derive ~~the~~ an adjustable delay signal, wherein the first selected phased signal, the second selected phased signal, and at least one selected phase information signal are received into the phase mixer, wherein at least one simulated phase signal is selected as an adjustment to the synchronizing signal.

Please amend claim 27 as follows:

27. An interface circuit for processing an input signal, comprising:

a phase locked loop (PLL) circuit adapted to generate a plurality of phased signals from a synchronizing signal that is associated with the input signal;

a phase adjuster adapted to generate an adjustable delay signal from two of the plurality of phased signals, wherein the phase adjuster includes:

a phase mixer, including:

at least three differential pairs, wherein a first one of the differential pairs is arranged to multiply a first selected phased signal with a first weight and a second one of the differential pairs is arranged to multiply a second selected phased signal with a second weight, and wherein the phase mixer is configured to activate two differential pairs from the at least three differential pairs to derive the adjustable delay signal,

wherein at least one simulated phase signal is selected as an adjustment to the synchronizing signal.

Please amend claim 33 as follows:

33. The circuit of claim 1, further comprising:

an analog to digital converter adapted to improve processing of the ~~analog color~~ input signal by choosing an adjustment to the delay signal~~, wherein at least one simulated phase signal is provided~~.

Allowable Subject Matter

3. The following is an examiner's statement of reasons for allowance:

Regarding claims 1, 5 and 11, the primary reason for allowance is the combination of the phase mixer receiving the first and second selected phases and a phase information signal and then adding different weights to the first and second phased signals and using these signals to arrive at the delay signal, in combination with the other recited limitations, which are not found singularly or in combination in the prior art.

The closest available references for teaching this phase mixer is Ward et al. (US 2004/0135602) and Donnelly et al. (US 2004/0223571). Ward et al. disclose of receiving

multiple phased signals and using two of these signals to derive a delay signal, however, does not teach of adding different weights to the first and second phased signals. Donnelly et al. disclose of receiving two phased signals, adding weights to these signals and deriving a delay signal from the two phase signals, however, Donnelly et al. fail to teach of the phase mixer receiving a phase information signal.

Regarding claim 13, the primary reason for allowance is the combination of deriving the delay signal from two of the plurality of phased signals by providing at least one simulated phase information signal, and multiplying a first and second one of the selected phased signals with a first and second weights, respectively, wherein the first and second weights are based, at least in part, on the at least one selected phase information signal, in combination with the other recited limitations, which are not found singularly or in combination in the prior art.

Regarding claim 27, the primary reason for allowance is the combination of the phase mixer including at least three differential pairs, wherein a first one of the differential pairs is arranged to multiply a first selected phased signal with a first weight and a second one of the differential pairs is arranged to multiply a second selected phased signal with a second weight, and wherein the phase mixer is configured to activate two differential pairs from the at least three differential pairs to derive the adjustable delay signal, in combination with the other recited limitations, which are not found singularly or in combination in the prior art.

Regarding claim 34, the primary reason for allowance is the combination of the a phase adjuster including a Phase Digital to Analog Converter, including a first current source circuit; a second current source circuit; and a third current source circuit, wherein the Phase Digital to Analog Converter is arranged to provide a first weight, based at least in part on the first weight signal and to provide a second weight, based at least in part on the second weight signal; and a phase mixer for multiplying a first selected phased signal with the first weight, multiplying a second selected phased signal with the second weight, and adding together the first and the second multiplied phased signals to derive the adjustable delay signal, in combination with the other recited limitations, which are not found singularly or in combination in the prior art.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

21 May 2007

AMR A. AWAD
SUPERVISORY PATENT EXAMINER